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Universal SPI Pin header
For BIOS tools series

This document aims to standardize the SPI Pin header over the different motherboard projects and platforms to benefit of all the BIOS solutions for development, production and repairing with a unique connector:

- ***Update the On board BIOS***
- ***Boot from a Backup Memory***
- ***Emulate the BIOS memory for very fast update (less than 3 seconds)***
- ***Debug your motherboard through SPI bus***
- ***Display POST messages from SPI bus before and after production***

Table of content:

I. Background

While SPI flash is soldered on the Motherboard, engineers need a way to update the bios codes without unsoldering the SPI flash part. With the increasing SPI Flash densities requirement for the BIOS codes (UEFI, advanced features..) Bios developers need optimized tools to reduce the time spent on bios code update or BIOS debugging.

Furthermore, some buses used for BIOS POST messages disappear (LPC connector, Com port, PCI slot) and some others require too heavy BIOS resources to be kept after production for RMA (USB) or are unstable. Development engineers, production, repairing service need an alternative way to access the Bios debug post messages.

All the above requirements can be fulfilled by using the SPI Bus designing a common 2*5 or 2*4 pin headers on the Motherboard.

II. SPI Universal Pin Header

The SPI Universal Pin Header is recommended to offer a full compatibility with all the BIOS tools solutions and avoid confusion over the motherboards and platforms. According to the features supported by the hardware, the pins can be connected to the signals or left unconnected. The pin header can be 2*5 or even 2*4.

Table 1: SPI Universal Pin Header

Signals name	Pins		Signals name
Hold2	**1**	**2**	**CS2**
CS1	**3**	**4**	**Vcc**
MISO	**5**	**6**	**Hold1**
IO3	**7**	**8**	**CKL**
GND	**9**	**10**	**MOSI**

Table 2: SPI Universal Pin Header

Pins	Signals name	Description
4	**Vcc**	**The Vcc pin must be connected to the SPI Flash Vcc.** - **SF100** supplies the BIOS memory if update is performed with motherboard not supplied - SPI Flash Vcc supplies **BBF** and **SPI POST card** tools - SPI Flash memory level is monitored by **EM100** during emulation
9	**GND**	**The GND is the common ground between motherboard and BIOS tools**
5, 8, 10	**CKL, MOSI, MISO**	**These 3 SPI Signals must be common in case motherboard is using 2 SPI Flash**
3	**CS1**	**Pin 3 is connected to Chip Select of SPI flash 1**

6	**Hold1**	The **Hold signal of SPI Flash 1** must be connected to the pin 6 for the tools to disable the on board SPI Flash 1 (**BBF, EM100, SPI POST Card**). Hold signal must be pulled high by a resistor in the application.
7	**IO3**	**IO3 is automatically driven low by SF100** in order to reset the system, turn OFF SPI isolation MOSFET or Switches. If In Circuit Programming is not supported by the application or if IO3 is not needed, Pin 7 can be kept unconnected.
2	**CS2**	Pin 2 is connected to **Chip Select of SPI flash 2** when motherboard is using two Serial Flash. The SPI Bus (CKL, MOSI and MISO) must be in common with SPI Flash 1
1	**Hold2**	Pin 1 is connected to **Hold signal of the SPI Flash 2** for the tools to disable the on board SPI Flash 2 (**BBF, EM100, SPI POST Card**). If the Hold signal of SPI Flash 2 is common with Hold signal of SPI Flash 1 or if there is only one SPI Flash then Pin1 can be removed and used has a mistake proof pin to prevent from wrong connections.

The universal pin header can therefore present different configuration according to the application scenarios but stay compatible with all the BIOS tools solutions:

1. Dual SPI Flash with In circuit programming

Hold2	**1**	**2**	**CS2**
CS1	**3**	**4**	**Vcc**
MISO	**5**	**6**	**Hold1**
IO3 or NC	**7**	**8**	**CKL**
GND	**9**	**10**	**MOSI**

2. Dual SPI Flash with common Hold signal

Mistake proof pin	**1**	**2**	**CS2**
CS1	**3**	**4**	**Vcc**
MISO	**5**	**6**	**Hold1**
NC	**7**	**8**	**CKL**
GND	**9**	**10**	**MOSI**

3. Single SPI Flash with In circuit programming

Mistake proof pin	**1**	**2**	**NC**
CS1	**3**	**4**	**Vcc**
MISO	**5**	**6**	**Hold1**
IO3 or NC	**7**	**8**	**CKL**
GND	**9**	**10**	**MOSI**

4. Single SPI Flash

Mistake proof pin	**1**	**2**	**NC**
CS1	**3**	**4**	**Vcc**
MISO	**5**	**6**	**Hold1**
NC	**7**	**8**	**CKL**
GND	**9**	**10**	**MOSI**

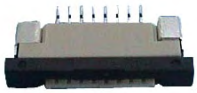
Cases 3 and 4 can also be replaced by a 4*2 Pin header

CS1	**1**	**2**	**Vcc**
MISO	**3**	**4**	**Hold1**
IO3 or NC	**5**	**6**	**CKL**
GND	**7**	**8**	**MOSI**

- **NC** is used for “Pin Not Connected” to any signals
- **Mistake proof pin** is used to prevent from Wrong connection. No pin is soldered on the board and the corresponding hole of the female connector must be filled by user.

2.54mm Pitch Pin header

1.27mm Pitch Pin header

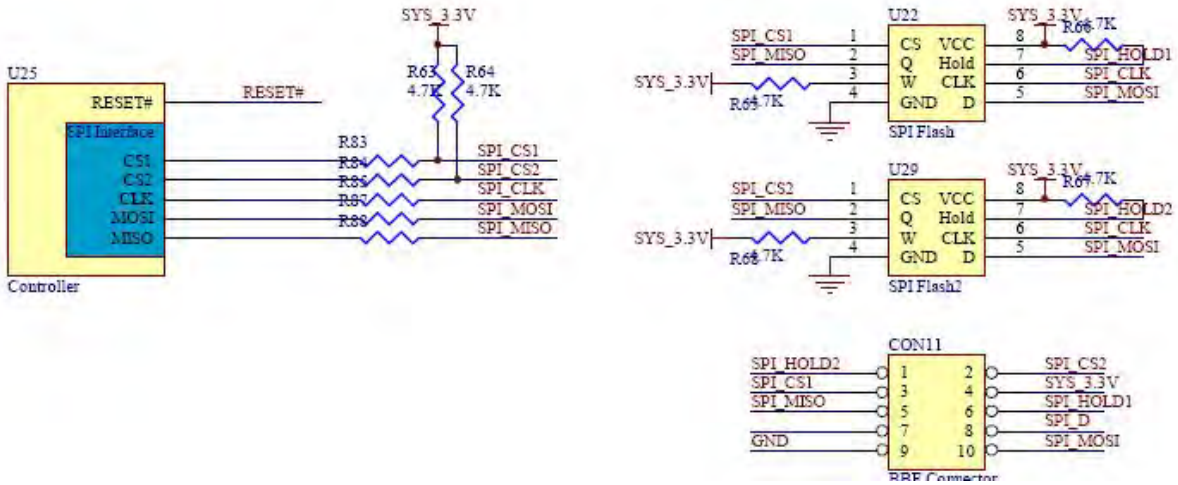


FPC 1.0 SMT (Laptop)

Please contact us for FPC connector solution

III. Schematics suggestions

Schematic 1: Dual SPI Flash

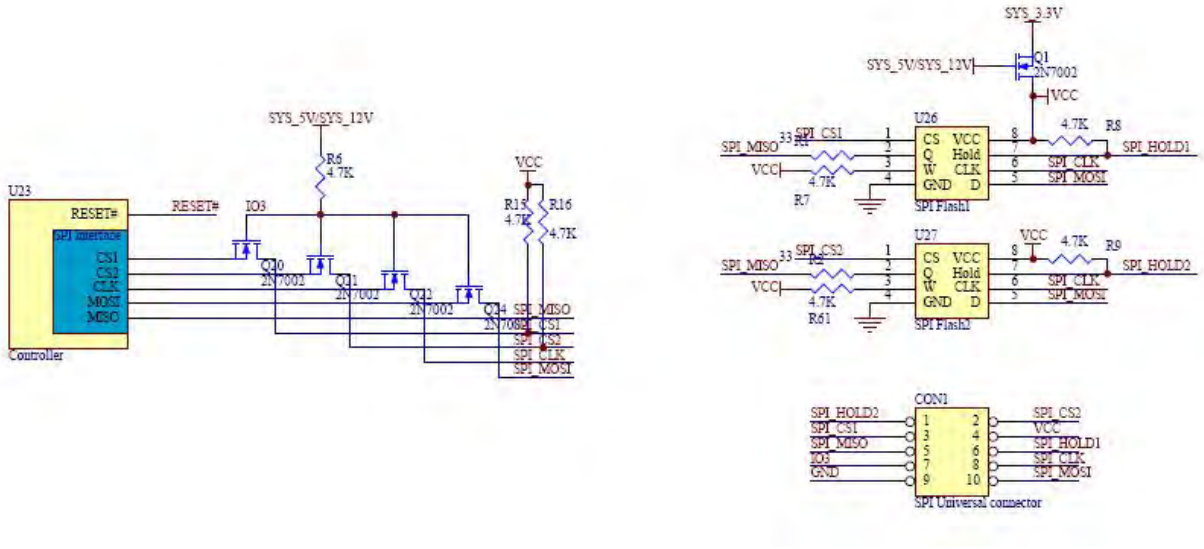


Remark 1: if the controller can switch the SPI output in High impedance when in Reset then IO3 of pin 7 can be connected to the system reset to use SF100 for In circuit programming.

Remark 2: if the Hold signals of both Serial Flash are in common then Pin 1 of pin header can be used as a mistake proof pin to prevent wrong connection (pin not soldered).

Remark 3: If motherboard is using only one SPI Flash, the connector can be reduced to 4*2

Schematic 2: Dual SPI Flash with In Circuit Programming



Remark 1: If motherboard is using only one SPI Flash, the connector can be reduced to 4*2

Please review Application note AN0103 for more detailed information on the In Circuit Programming hardware implementation and the different solutions.

IV. BIOS solutions supported

1. Motherboard boots from back up SPI Flash

DediProg tools can force the motherboard to boot from backup memories by disabling the on board Serial Flash (Hold signals driven low).

Tools support:

- Backup Boot Flash (BBF) ➔ Pin out compatible with “SPI Universal Header”
- EM100 (Emulator) ➔ Pin out compatible with “SPI Universal Header”
- SPI POST Card (RMA) ➔ Pin out compatible with “SPI Universal Header”

Benefits:

- **BIOS Development:** The backup Serial Flash can be safely updated without any possible conflict with the application controller (Chipset or Embedded controller).
- **Recover from corrupted Bios (RMA):** Motherboard with corrupted BIOS can be boot from a backup BIOS Flash with good BIOS. After boot, the on board SPI Flash BIOS can be updated by using the Flash utility tool.

2. Direct update of the on board SPI Flash

DediProg programmers can directly update the BIOS of the on board SPI Flash if the motherboard hardware can support In Circuit Programming.

Tools support:
- SF100 (USB programmer) ➔ Adaptor board needed
- SF300 (USB and Stand Alone Programmer) ➔ Adaptor board needed

Benefits:
- **BIOS Development:** Flash the on board BIOS with high performance
- **Production:** Program the SPI Flash on board with the production Tester (ICT)
- **Recover from corrupted Bios (RMA):** Motherboard corrupted BIOS can be flashed with good BIOS in the field.

Please contact DediProg to order the adaptor board from "SF100 pin out" to "SPI Universal pin out".

3. BIOS update in less than 3 seconds

DediProg SPI Flash Emulator can emulate any market SPI flash. The RAM base memory of the emulator can be updated (erased, programmed and Verify) in less than 3 seconds (from 512Kb to 128Mb). The on board SPI Flash will be disabled and the motherboard will boot from the emulator.

Tools support:
- EM100 (SPI Flash emulator) ➔ Pin out compatible with "SPI Universal Header"

Benefits:
- **BIOS Development:** very fast BIOS update for development time.

4. Collect SPI protocol trace during boot process

System boot can be analyzed by connecting our SPI bus analyzer to the "SPI Universal Header". The SPI Trace will be helpful for a low level debugging of the boot.

Tools support:
- EM100 (SPI bus analyzer) ➔ Pin out compatible with "SPI Universal Header"

Benefits:
- **Chipset development:** SPI interface debugging
- **BIOS Development:** SPI protocol debugging
- **Platform testing:** the SPI trace can be saved during motherboard power cycling for analysis.

5. Display debug POST messages through SPI bus

Sending post messages through SPI bus become an efficient way of collecting debug messages as:
1) SPI bus is always available on any platform
2) SPI bus is available earlier than others Serial Bus (USB) during boot process
3) SPI bus POST messages are lighter to be implemented in the BIOS than others serial Bus (USB) and can be kept in production for field debug.

Tools support:

- EM100 (POST messages display on host PC)
  ➔ Pin out compatible with "SPI Universal Header"
- SPI POST Card ((POST messages display on segment LED or LCD)
  ➔ Pin out compatible with "SPI Universal Header"

Benefits:

- **BIOS Development:** Possibilities to customize all the POST messages (variable output, timing..)
- **Repairing (Field):** SPI POST is universal as SPI bus is available on all the platforms

Ask for DediProg SPI Hyper terminal specification and BIOS sample code.

6. BIOS Debugger

EM100 can be used as a bidirectional SPI Bridge between the Host PC and the target system. By customizing the GUI on the host PC and the BIOS on the target motherboard, Engineers can use EM100 as a BIOS Debugger and control from the Host PC his target system (POST, System information, Chipset/CPU registers, memories, timing etc..).

Tools support:

- EM100 (Bidirectional communication between Host PC and BIOS)
  ➔ Pin out compatible with "SPI Universal Header"

Benefits:

- **BIOS Development:** powerful BIOS debugger, stable in any platform and customizable.

Ask for DediProg SPI Hyper terminal specification, software .DLL or DediProg customization support.

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